SILIGURI INSTITUTE OF TECHNOLOGY

DEPARTMENT OF ECE

1st Internal Examination (CA2) – May 2021

PAPER NAME: **CMOS VLSI DESIGN** PAPER CODE: **PE-EC603C**

FULL MARKS: 30 TIME: 1Hour

I. ANSWER ALL QUESTIONS (5X1 = 5)

(1) LUT is used in

i) CPLD ii) FPGA iii) SPLD iv) ASIC

(2) In a PLA which one is programmable?

i) AND plane ii) OR plane iii) Both AND & OR plane iv) None

(3) FPGA is a

i) Full Custom ASIC ii) Semi Custom ASIC iii) Programmable ASIC iv) Both (ii) & (iii)

(4) PAL and PLA are known as

i) CPLD ii) SPLD iii) FPLD iv) GPLD

(5) Which one of the following is not considered as an ASIC?

i) IC for an electronic guitar ii) Network Interface chip iii) DRAM iv) IC for Bluetooth application

Group A: ANSWER ANY ONE (Based on CO1) (1X5=5)

Q1. Draw Y - Chart and explain VLSI Design Flow.

Q2. Explain the gate array based VLSI system design.

Group B: ANSWER ANY ONE (Based on CO2) (1X5=5)

Q1. Discuss the layout design rules.

Q2. What is Stick Diagram? Draw the Stick Diagram of CMOS Inverter.

Group C: ANSWER ANY ONE (Based on CO2) (1X15=15)

Q1. Explain the Basic Steps of Fabrication Process.

Q2. Design a Full Adder Circuit using PAL.